REMARKS

The Office Action mailed on November 24, 2003, has been carefully reviewed and the foregoing amendments and following remarks are offered in response thereto. Applicants respectfully request favorable reconsideration of this application, as amended.

Claims 1-3 and 15-17 have been canceled without prejudice to the underlying subject matter, and claims 21-24 have been added. Claims 4, 5 and 8 have been amended to correct the informalities noted in the Examiner's objection. Claim 7 has been amended to overcome the Examiner's rejection under 35 U.S.C. § 112, second paragraph. Without acceding to the rejections under 35 U.S.C. §§ 102(b) and 103(a), claims 4-14 have been amended to correct various informalities and to clarify certain features of the claimed invention. Thus, claims 4-14 and 21-24 are pending.

The Examiner's indication of allowable subject matter in Claims 10, 11 and 14 is noted with appreciation. Those claims have been re-written as claims 22, 23 and 24, respectively.

Applicants submit that the rejections under 35 U.S.C. §§ 102(b) and 103(a) are inappropriate, at least insofar as

those rejections are considered vis-à-vis the claims as now pres nted.

Claims 4, 5 and 7, as amended, are directed to a trench-gate type semiconductor device and recite, *inter alia*, a contact hole extending from a second semiconductor region into a first semiconductor region and a side wall spacer formed on a side wall of a gate pillar. The contact hole is formed by an etching process using the side wall spacer as a mask. The art relied upon in the rejections does not teach or suggest the features recited in independent claims 4, 5 and 7.

Lu is directed to a method for making a vertical DRAM cell which includes a vertical channel field effect transistor having a gate electrode, source/drain elements and a capacitor. Lu discloses that openings 50 extend through insulating dielectric layer 34 to contact source/drain regions 30. Lu fails to teach or suggest that openings 50 extend from a semiconductor source region, such as source/drain region 30, to a semiconductor channel region, such as substrate layer 12.

Furthermore, Lu discloses that mask 40 and spacer 42 are used to etch openings 50 in insulating dielectric layer 34, after which mask 40 and spacer 42 are removed. Lu fails to teach or suggest that dielectric spac r layer 32,

located on the sidewalls of layer structures 24 and 28, may be used as an etching mask. *See*, e.g., Col. 2, lines 20-49; Col. 6, lines 7-22; FIGS. 8A, 8B, 9A and 9B. Moreover, the secondary references relied upon in the rejections under 35 U.S.C. § 103(a) do not cure the deficiencies of Lu with respect to claims 4, 5 or 7.

Claim 8 is directed to a trench-gate type semiconductor device and recites, *inter alia*, a first plurality of trenches which penetrates a first semiconductor region and extends from a major surface of a second semiconductor region into a semiconductor main body, and a second plurality of trenches, shallower than the first plurality of trenches, extending from the major surface of the second semiconductor region into the first semiconductor region. The second plurality of trenches are located between adjacent side wall spacers.

The rejection of claim 8 under 35 U.S.C. § 103(a) proposes to combine the teachings of Lu and Huang "to make alignment easier." The proposed combination of these references is inappropriate. Moreover, even if the teachings of the references were appropriately combined, the combination would not teach or suggest the invention of claim 8.

The rejection of claim 8 refers to "a plurality of secondary trenches which are made shallower than said first trenches (Huang shows these trenches to be either shallower (figures 9 and 11) or deeper (figure 13), and are formed in such a manner that said secondary trenches are reached from the major surface of the second semiconductor region to said first semiconductor region between said side wall spacers located adjacent to each other."

Lu fails to disclose a second plurality of trenches shallower than the first plurality of trenches, and, furthermore, suggests no motivation to do so. While Huang discloses a first trench, i.e., trenches 20, 22, and a second trench, i.e., trench 34, Huang fails to disclose whether layer of polysilicon 26, filling trenches 20, 22, or metal layer 36, filling trench 34, may include projecting gate pillars, or side wall spacers formed on projecting gate pillars. Similarly, Huang fails to teach or suggest that trench 34 may be located between adjacent gate pillar side wall spacers. *See*, e.g., FIG. 8; Col. 2, lines 39-43. Accordingly, Applicants respectfully submit that the Office is apparently engaging in impermissible hindsight reconstruction to combine these references to allegedly arrive at the claimed invention. Moreover, the secondary references relied upon in the rejections under 35

U.S.C. § 103(a) do not cure the deficiencies of Lu and Huang with respect to claim 8.

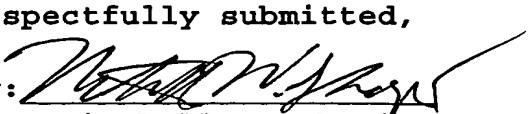
As is apparent, none of the references of record teaches or suggests the above-identified features nor is capable of providing the exemplary advantages discussed in the specification associated with the claimed trench-gate type semiconductor device.

In view of the amendments presented herein, and the reasons explained in the preceding remarks, Applicants submit that this application is in condition for allowance and should now be passed to issue.

A Notice of Allowance is respectfully solicited.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

By: 

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